CLAIMS

What is claimed is:

1. A system comprising:

a processor; and

a memory device operatively coupled to the processor, the memory device comprising a plurality of vertically stacked ball grid arrays, each ball grid array having a memory chip.

2. The system, as set forth in claim 1, wherein the vertically stacked ball grid arrays comprise:

a plurality of packages, each of the plurality of packages physically coupled to another of the plurality of packages; and

a plurality of memory chips, each of the plurality of memory chips physically coupled to a respective one of the plurality of packages.

3. The system, as set forth in claim 2, wherein each package comprises:

a molded resin body having a die side and a wire side.

4. The system, as set forth in claim 3, wherein each package comprises:

a plurality of first alignment features on the die side of the package; and

a plurality of second alignment features on the wire side of the package.

5. The system, as set forth in claim 4, wherein the plurality of first alignment features are male and the plurality of second alignment features are female.

6. The system, as set forth in claim 4, wherein the plurality of first alignment features are male and the plurality of second alignment features are male.

7. The system, as set forth in claim 4, wherein the plurality of first alignment features are female and the plurality of second alignment features are male.

8. The system, as set forth in claim 4, wherein the plurality of first alignment features are female and the plurality of second alignment features are female.

9. The package, as set forth in claim 4, wherein the plurality of first alignment features and the plurality of second alignment features orient adjacent packages in a unique location.

10. The package, as set forth in claim 9, wherein the plurality of first alignment features and the plurality of second alignment features are arranged asymmetrically.

11. The package, as set forth in claim 9, wherein the plurality of first alignment features and the plurality of second alignment features comprising of at least one unique alignment feature.

12. The package, as set forth in claim 4, wherein the plurality of first alignment features and the plurality of second alignment features support adjacent packages during solder ball reflow.

13. The system, as set forth in claim 2, wherein each of the plurality of packages is electrically coupled to another of the plurality of packages using solder balls.

14. The system, as set forth in claim 13, wherein each of the plurality of packages comprise vias extending therethrough to connect solder balls of adjacent packages serially.

15. A memory board comprising:

a substrate; and

a memory device operatively coupled to the substrate, the memory device comprising a plurality of vertically stacked ball grid arrays, each ball grid array having a memory chip.

16. The memory board as set forth in claim 15, wherein the substrate is a printed circuit board.

17. The memory board, as set forth in claim 15, further comprising a memory controller operatively coupled to the memory device and to the substrate.

18. The memory board, as set forth in claim 15, wherein the stacked ball grid array comprises:

a plurality of packages, each of the plurality of packages coupled to another of the plurality of packages; and

a plurality of memory chips, each of the plurality of memory chips coupled to a respective one of the plurality of packages.

19. The memory board, as set forth in claim 18, wherein the package comprises:

a molded resin body having a die side and a wire side.

20. The memory board, as set forth in claim 19, wherein the molded resin package comprises:

a plurality of first alignment features on the die side of the package; and

a plurality of second alignment features on the wire side of the package.

21. The memory board, as set forth in claim 20, wherein the plurality of first alignment features are male and the plurality of second alignment features are female.

22. The memory board, as set forth in claim 20, wherein the plurality of first alignment features are male and the plurality of second alignment features are male.

23. The memory board, as set forth in claim 20, wherein the plurality of first alignment features are female and the plurality of second alignment features are male.

24. The memory board, as set forth in claim 20, wherein the plurality of first alignment features are female and the plurality of second alignment features are female.

25. The package, as set forth in claim 20, wherein the plurality of first alignment features and the plurality of second alignment features orient adjacent packages in a unique location.

26. The package, as set forth in claim 25, wherein the plurality of first alignment features and the plurality of second alignment features are arranged asymmetrically.

27. The package, as set forth in claim 25, wherein the plurality of first alignment features and the plurality of second alignment features comprising of at least one unique alignment feature.

28. The package, as set forth in claim 20, wherein the plurality of first alignment features and the plurality of second alignment features support adjacent packages during solder ball reflow.

29. The memory board, as set forth in claim 18, wherein each of the plurality of packages is electrically coupled to another of the plurality of packages using solder balls.

30. The memory board, as set forth in claim 29, wherein each of the plurality of packages comprise vias extending therethrough to connect solder balls of adjacent packages serially.

31. The memory board, as set forth in claim 15, wherein a first ball grid array is coupled to a second ball grid array.

32. The memory board, as set forth in claim 15, wherein the first ball grid array is serially coupled to the second ball grid array.

33. A stacked ball grid array.

34. The stacked ball grid array, as set forth in claim 33, wherein the stacked ball grid array comprises:

a plurality of packages, each of the plurality of packages coupled to another of the plurality of packages; and

a plurality of memory chips, each of the plurality of memory chips coupled to a respective one of the plurality of packages.

35. The stacked ball grid array, as set forth in claim 34, wherein the package comprises:

a molded resin body having a die side and a wire side.

36. The stacked ball grid array, as set forth in claim 35, wherein the molded resin package comprises:

a plurality of first alignment features on the die side of the package; and

a plurality of second alignment features on the wire side of the package.

37. The stacked ball grid array, as set forth in claim 36, wherein the plurality of first alignment feature are male and the plurality of second alignment features are female.

38. The stacked ball grid array, as set forth in claim 36, wherein the plurality of first alignment features are male and the plurality of second alignment features are male.

39. The stacked ball grid array, as set forth in claim 36, wherein the plurality of first alignment features are female and the plurality of second alignment features are male.

40. The stacked ball grid array, as set forth in claim 36, wherein the plurality of first alignment features are female and the plurality of second alignment features are female.

41. The package, as set forth in claim 36, wherein the plurality of first alignment features and the plurality of second alignment features orient adjacent packages in a unique location.

42. The package, as set forth in claim 41, wherein the plurality of first alignment features and the plurality of second alignment features are arranged asymmetrically.

43. The package, as set forth in claim 41, wherein the plurality of first alignment features and the plurality of second alignment features comprising of at least one unique alignment feature.

44. The package, as set forth in claim 36, wherein the plurality of first alignment features and the plurality of second alignment features support adjacent packages during solder ball reflow.

45. The stacked ball grid array, as set forth in claim 34, wherein each of the plurality of packages is electrically coupled to another of the plurality of packages using solder balls.

46. The stacked ball grid array, as set forth in claim 45, wherein each of the plurality of packages comprise vias extending therethrough to connect solder balls of adjacent packages serially.

47. A device comprising:

a chip; and

a package operatively coupled to the chip, the package comprising:

a first side;

a second side;

a plurality of first alignment features on the first side of the package; and

a plurality of second alignment features on the second side of the package.

48. The device, as set forth in claim 47, wherein the package comprises:

a molded resin body containing a die side and a wire side.

49. The device, as set forth in claim 47, wherein the plurality of first alignment features are male and the plurality of second alignment features are female.

50. The device, as set forth in claim 47, wherein the plurality of first alignment features are male and the plurality of second alignment features are male.

51. The device, as set forth in claim 47, wherein the plurality of first alignment features are female and the plurality of second alignment features are male.

52. The device, as set forth in claim 47, wherein the plurality of first alignment features are female and the plurality of second alignment features are female.

53. The device, as set forth in claim 47, wherein there are a plurality of memory chips, each of the plurality of memory chips coupled to a package.

54. A package comprising:

a first side;

a second side;

a plurality of first alignment features on the first side of the package; and

a plurality of second alignment features on the second side of the package.

55. The package, as set forth in claim 54, wherein the package comprises:

a molded resin body.

56. The package, as set forth in claim 54, wherein the plurality of first alignment features are male and the plurality of second alignment features are female.

57. The package, as set forth in claim 54, wherein the plurality of first alignment features are male and the plurality of second alignment features are male.

58. The package, as set forth in claim 54, wherein the plurality of first alignment features are female and the plurality of second alignment features are male.

59. The package, as set forth in claim 54, wherein the plurality of first alignment features are female and the plurality of second alignment features are female.

60. The package, as set forth in claim 54, wherein the plurality of first alignment features and the plurality of second alignment features orient adjacent packages in a unique location.

61. The package, as set forth in claim 60, wherein the plurality of first alignment features and the plurality of second alignment features are arranged asymmetrically.

62. The package, as set forth in claim 60, wherein the plurality of first alignment features and the plurality of second alignment features comprising of at least one unique alignment feature.

63. The package, as set forth in claim 54, wherein the plurality of first alignment features and the plurality of second alignment features support adjacent packages during solder ball reflow.